

FIG. 1
(Prior art)

100

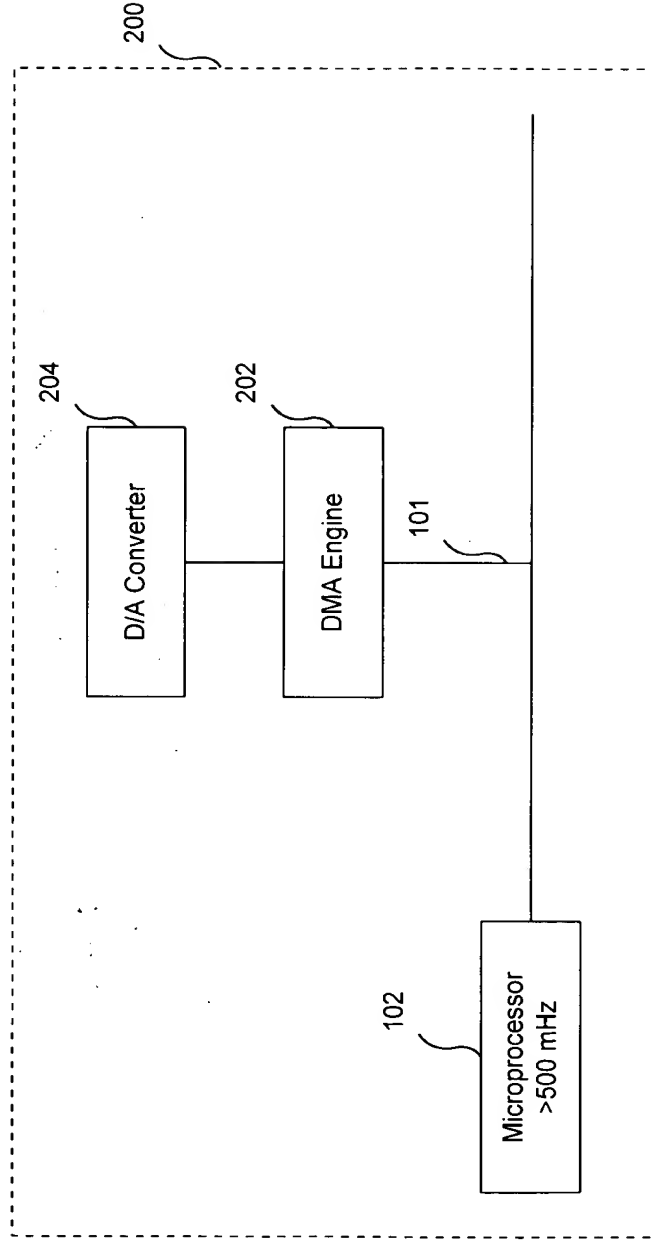
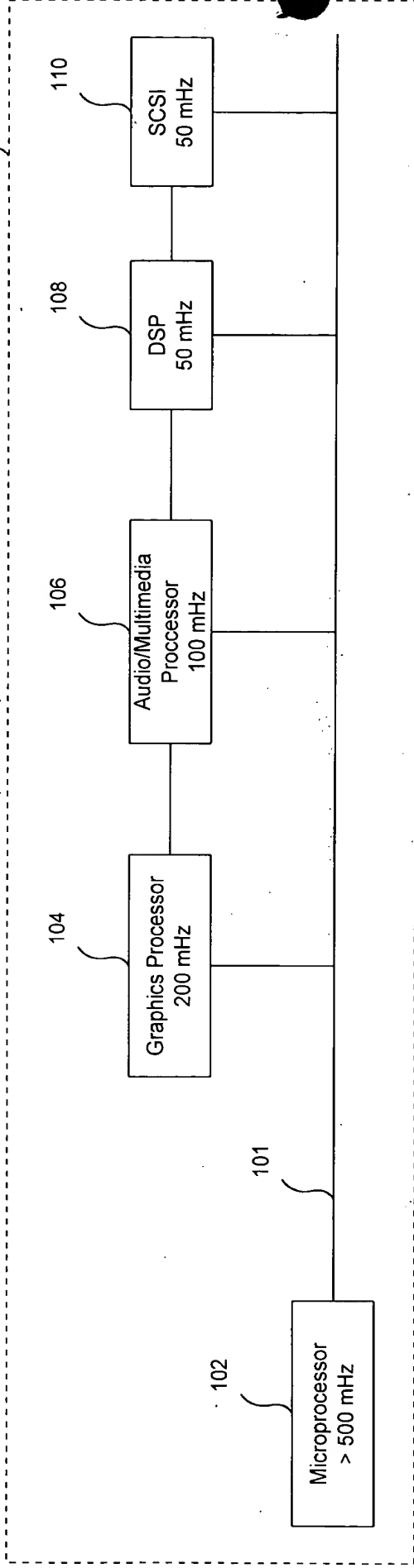


FIG. 2

300

SYSTEM PROCESSOR

L1 Cache

305

L2 Cache

System Bus

301

316

Memory

318

IM

Control Logic

320

CHIP SET 1

304

306

SDRAM

308

AGP

303

PCI BUS

310

CHIP SET 2

312

USB

314

SES1

FIG. 3

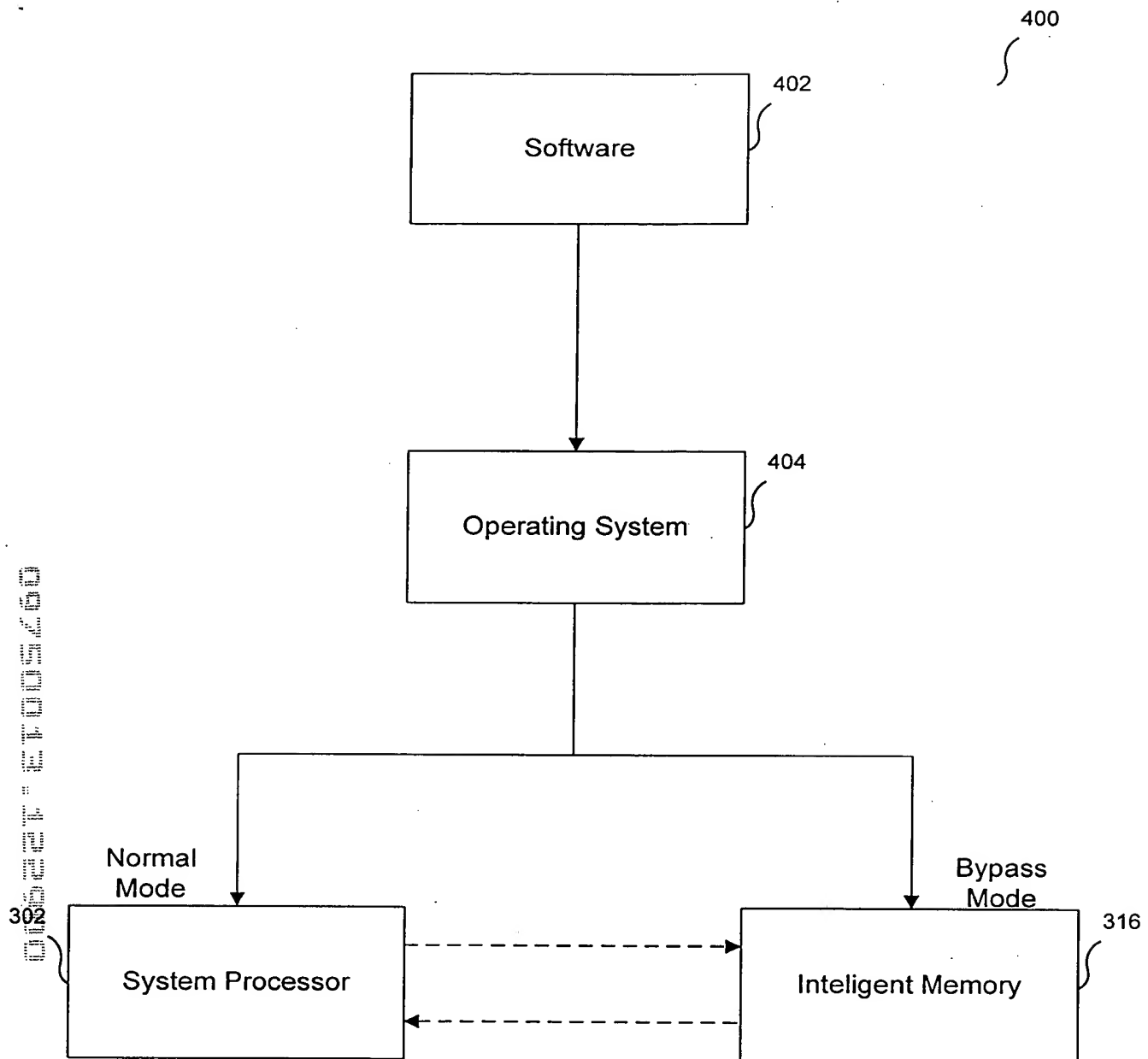


FIG. 4

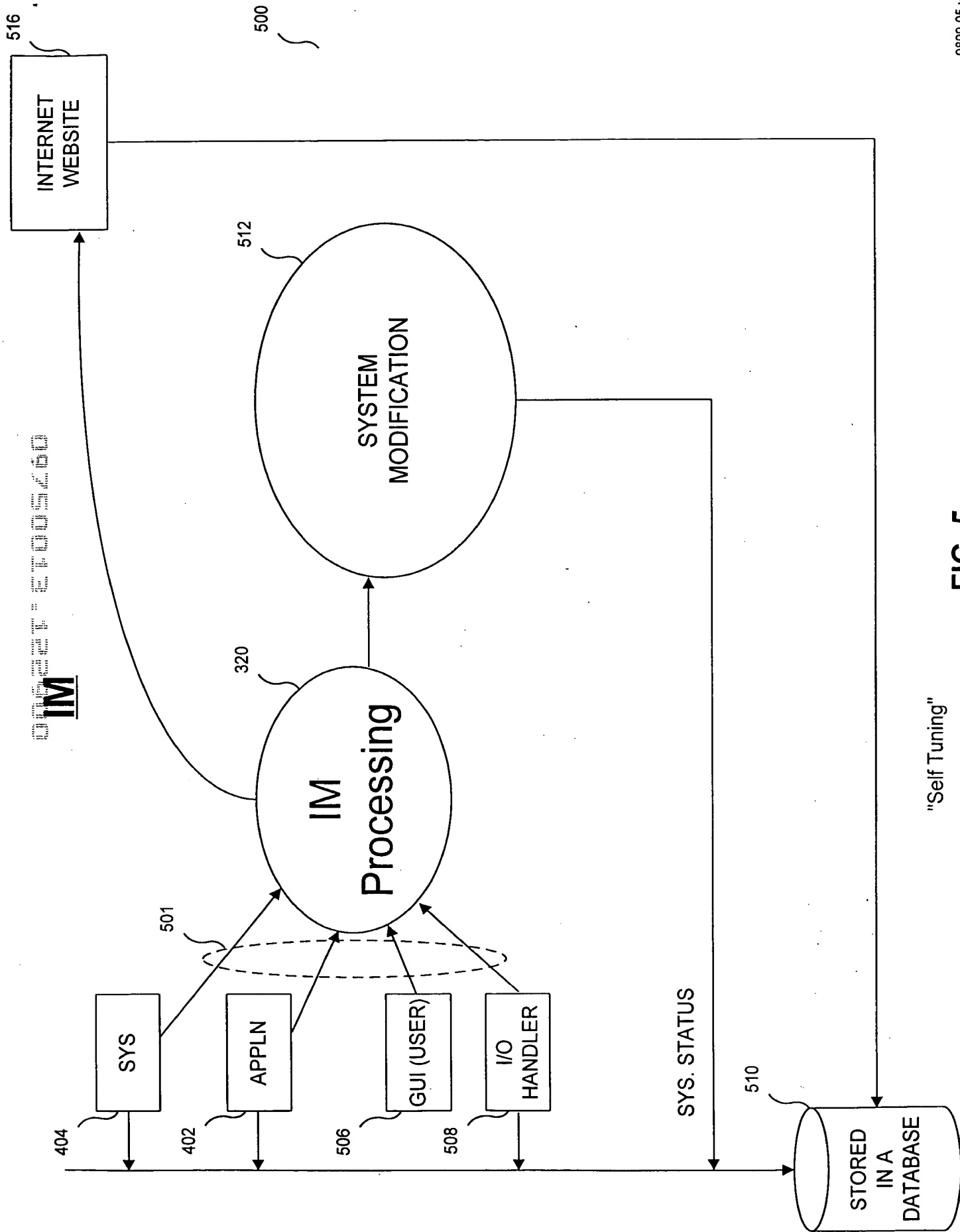


FIG. 5

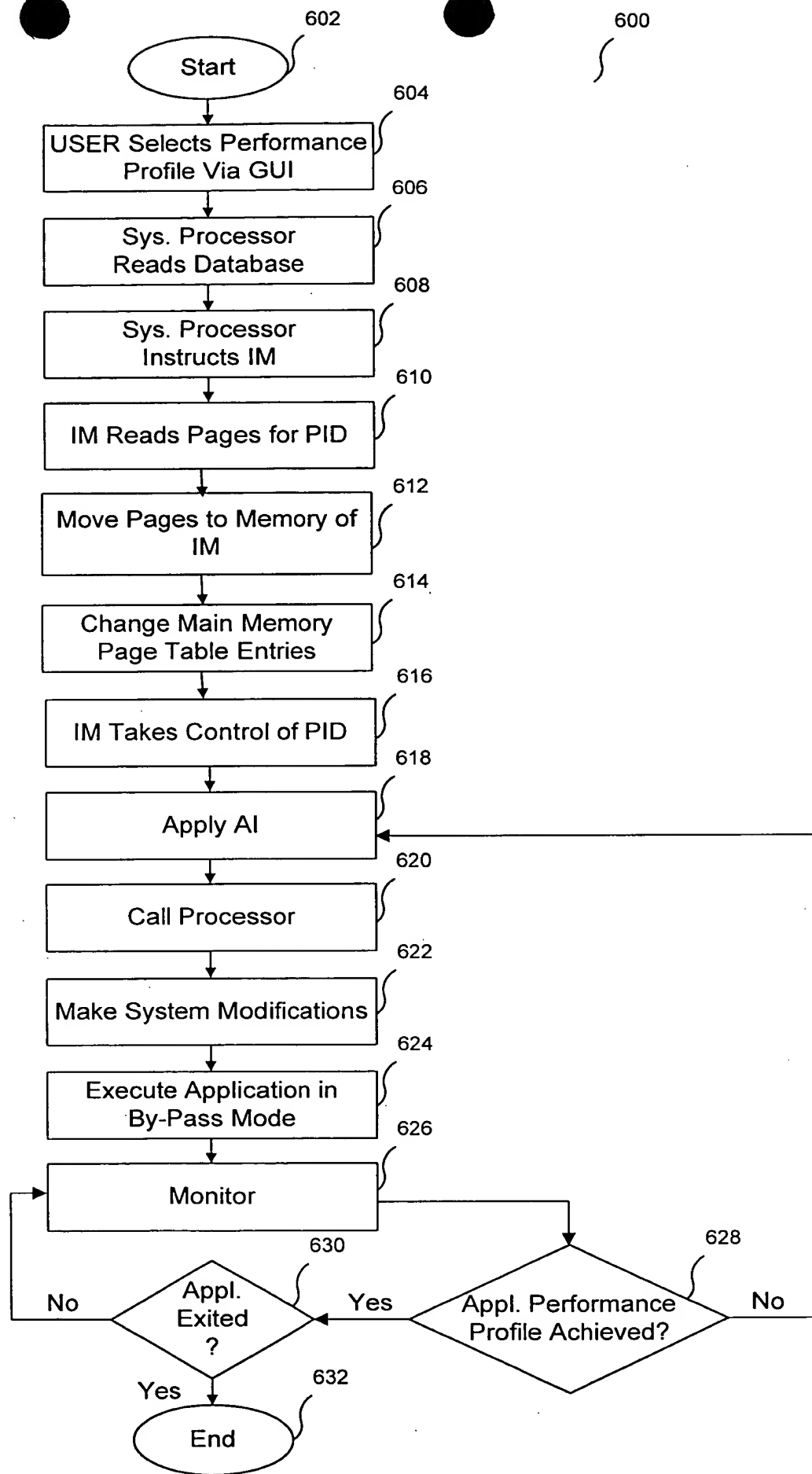
[illegible]

FIG. 6

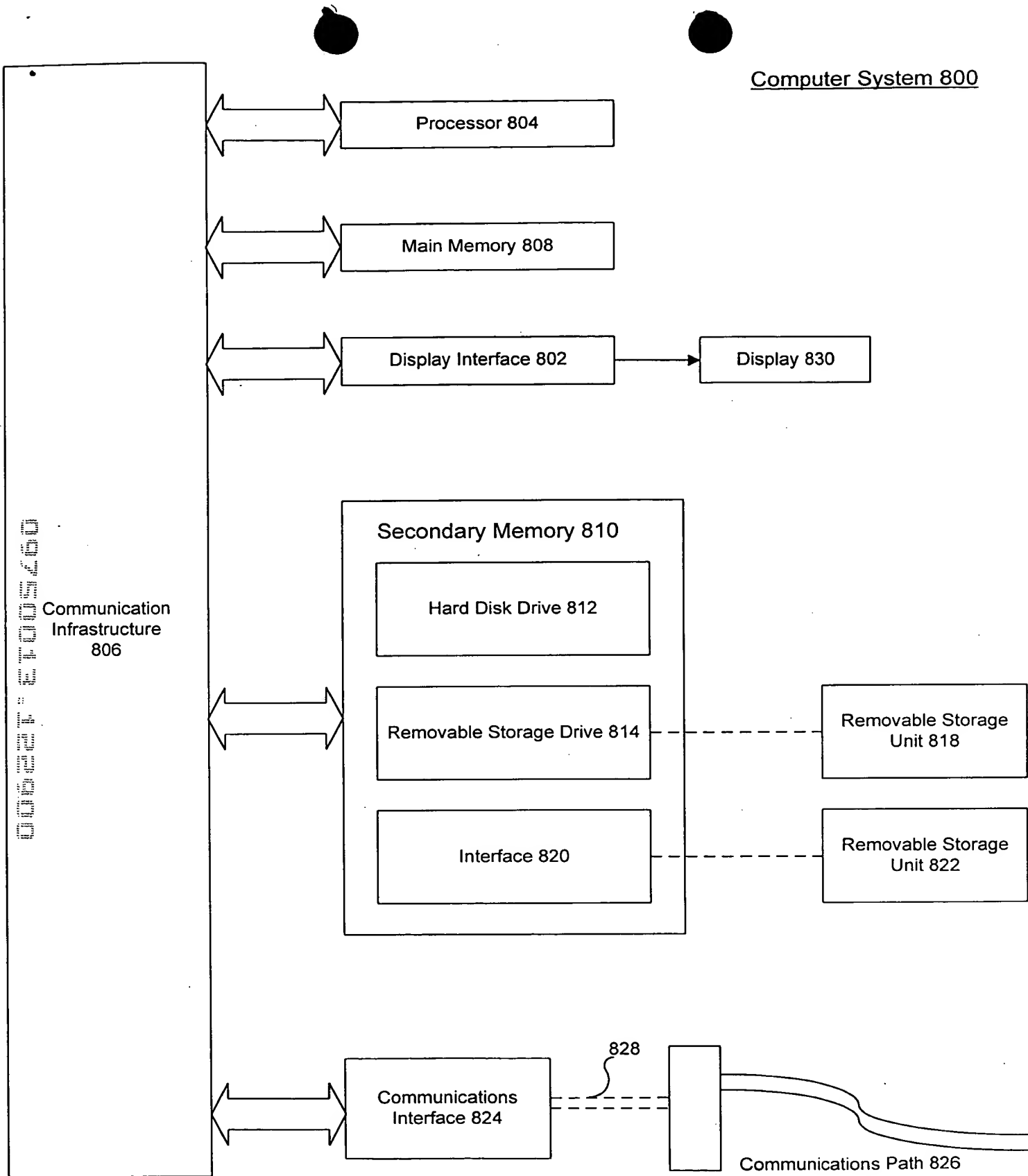


FIG. 8

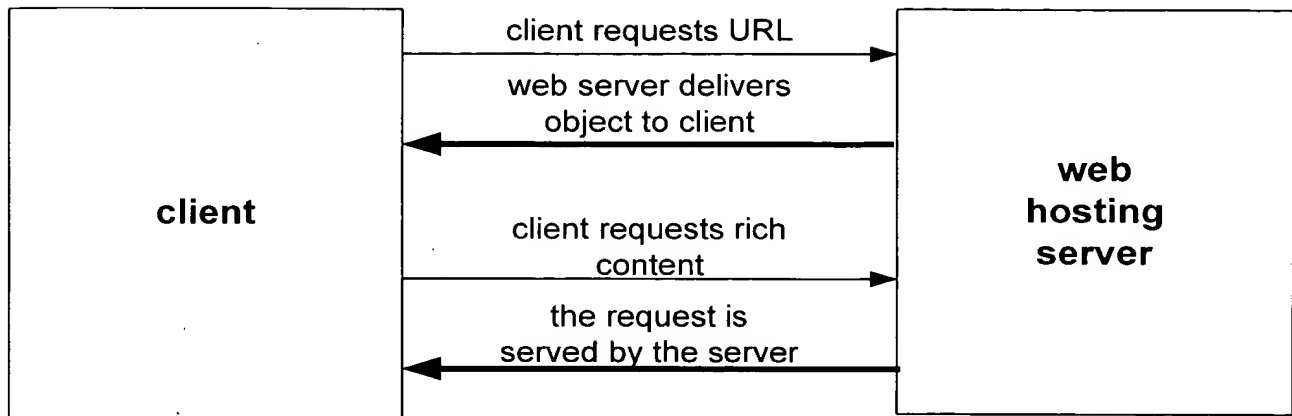


FIG. 9
(Prior art)

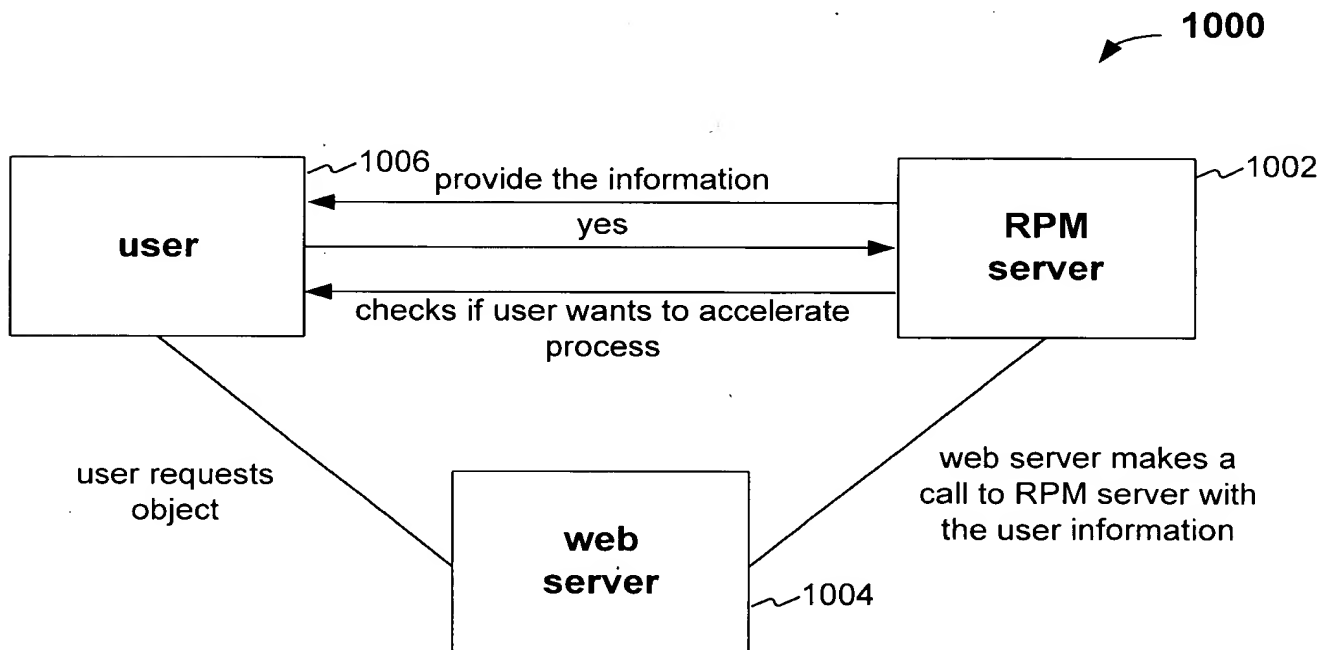
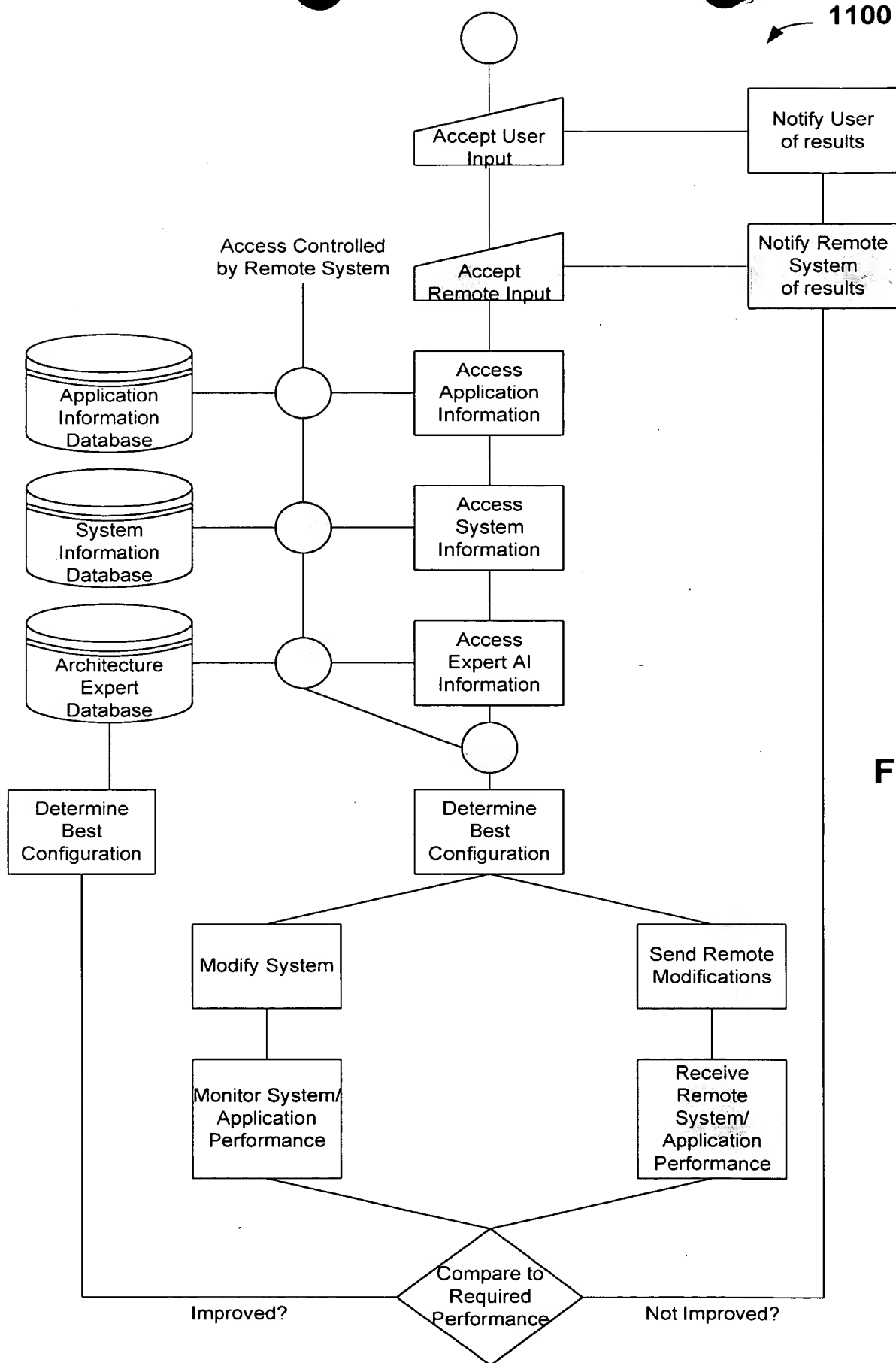


FIG. 10



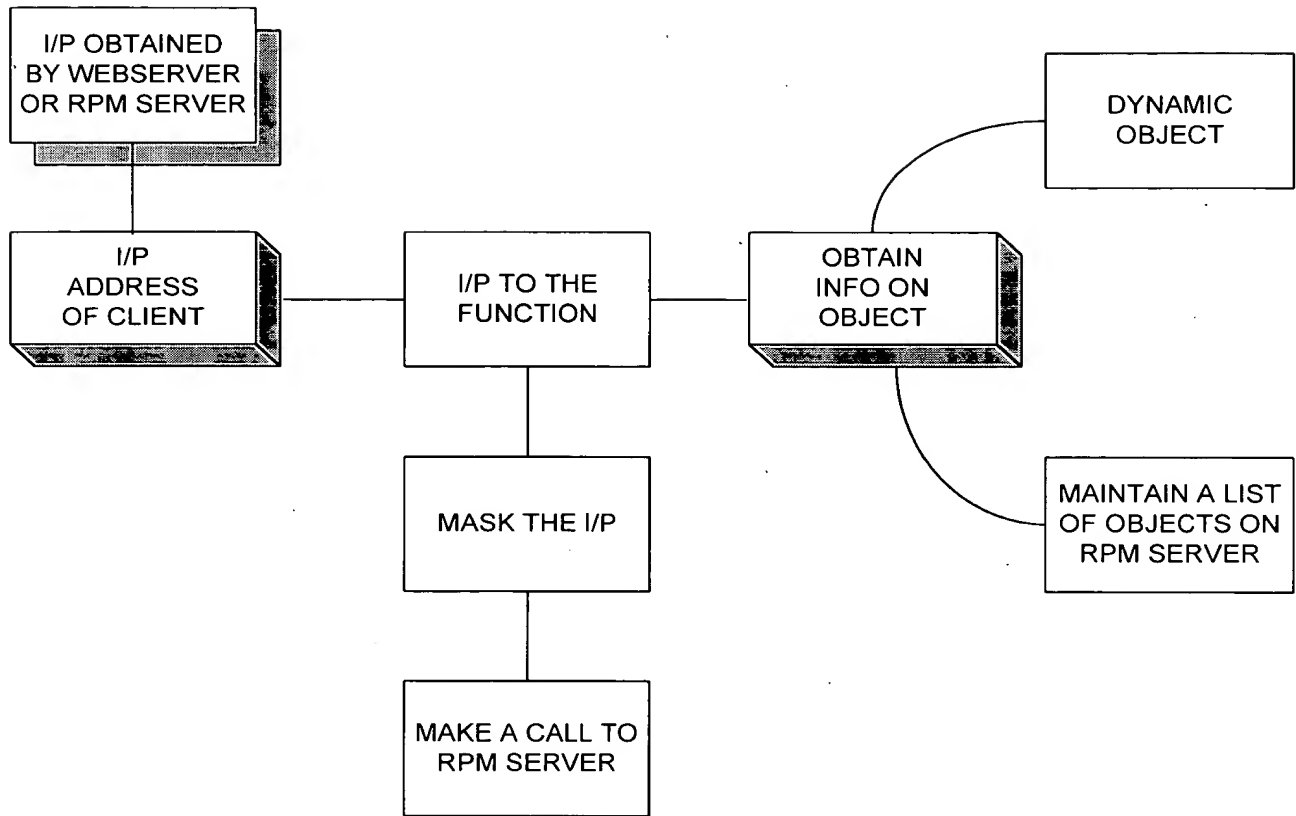


FIG. 12